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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/820,755 | 04/09/2004 | Masanao Yokoyama | 8019-1039 | 8776 |

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| EXAMINER | |
|---|---|
| ROSSOSHEK, YELENA | |
| **ART UNIT** | **PAPER NUMBER** |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/820,755 | YOKOYAMA, MASANAO | |
| | Examiner | Art Unit | |
| | Helen Rossoshek | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12,17,18 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,7,20-24 and 26* is/are allowed.

6)☒ Claim(s) *1-5,8-12,17,18 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to the Application 10/820,755 filed 04/09/2004 and amendment filed 04/09/2007.

2. Claims 1-12, 17, 18, 20-26 are pending in the Application. Claims 24-26 have been added to the Application.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/09/2007 has been entered.

### *Claim Objections*

4. Claims 9, 11 are objected to because of the following informalities: the limitation "wherein said first hard-macro includes a **plurality of said at least one** signal wire ..." is formulated unclear to what Applicant intent to mean.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5, 8-12, 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Ulrey (US Patent 6,642,556).

With respect to claim 1 Ulrey teaches a first hard-macro arranged on a semiconductor chip and constituting a part of a semiconductor integrated circuit that includes plural blocks and plural hard-macros other than the first hard-macro that are connected to each other with signal wires (within design of the integrated circuit comprising a plurality of macro cells places and routed creating a layout of the integrated circuit (col. 1, ll.27-31; ll.36-39; ll.49-51), wherein first macro C 2200 is arranged on the semiconductor chip, which is an one of the plural macros as shown on the Fig. 2 (col. 5, ll.1-3)),

including at least one signal wire passing through the first hard-macro, wherein the at least one signal wire is formed in the first hard-macro before the first hard-macro is arranged on the semiconductor chip (within interconnections 2220-2280 propagating signal paths inside of the macro C 2200, wherein interconnections are premapped before arranging on the layout (col. 5, ll.1-3; Fig. 2)), and

the at least one signal wire starts at a first outer edge of the first hard-macro and terminates at a second outer edge of the first hard-macro intersecting with the first outer edge (as shown on the Fig. 2 interconnections 2220-2280 start at one side of the macro C 2200 and terminate at a second side of the macro C 2200),

wherein the at least one signal wire is not a power supply line through which power is supplied to the semiconductor integrated circuit from a power supply (within

signal paths 2020-2090 to propagate signal through macro C2200 (col. 5, ll.5-7; ll.13-16; Fig. 2).

With respect to claim 12 Ulrey teaches a hard-macro arranged on a semiconductor chip and constituting part of a semiconductor integrated circuit (within design of the integrated circuit comprising a plurality of macro cells places and routed creating a layout of the integrated circuit (col. 1, ll.27-31; ll.36-39; ll.49-51), wherein first macro C 2200 is arranged on the semiconductor chip, which is an one of the plural macros as shown on the Fig. 2 (col. 5, ll.1-3)),

hard-macro comprising at least one wire passing through inside of the hard-macro and that starts at a first outer edge of the hard-macro and terminates at a second outer edge of the hard-macro intersecting with the first outer edge (within interconnections 2220-2280 propagating signal paths inside of the macro C 2200, wherein interconnections are premapped before arranging on the layout (col. 5, ll.1-3; Fig. 2)),

wherein the wire is divided into a plurality of portions each of which is arranged in each of a plurality of hierarchies of the hard-macro (as shown on the Fig. 2 by shifting them that they reach an adjacent side of the macro C 2200 (col. 5, ll.13-17), wherein the positions of each path are specifically chosen so that signal path 2020-2090 are automatically physically aligned between the signal source block 2000 at endpoints 2110-2180 (col. 5, ll.5-9)).

With respect to claims 2-5, 8-11, 25 Ulrey teaches:

Claims 2: wherein the first and second outer edges are adjacent to each other (as shown on the Fig. 2 (col. 5, ll.13-15);

Claim 3: wherein the first and second outer edges are perpendicular to each other (as shown on the Fig. 2 illustrating macro C 2200);

Claim 4: wherein the at least one signal wire is L-shaped (as shown on the Fig. 2 signal paths to be propagated are then shifted in L-shape illustrating macro C 2200);

Claim 5: wherein the at least one signal wire is linear (as shown on the Fig. 2 signal paths are linear illustrating macro C 2200);

Claim 8: further including a repeater inserted in the at least one signal wire (within incorporating a variety of signal modifiers, e.g. buffers (col. 4, ll.44-48));

Claim 9: wherein the first hard-macro includes a plurality of the at least one signal wires passing therethrough (within plurality of signal paths propagated through macro C (col. 5, ll.5-7));

Claim 10: wherein the pluralities of signal wires are equally spaced away from adjacent ones (as shown on the Fig. 2 illustrating macro C 2200)

Claim 11: wherein at least one of the plurality of signal wires includes a repeater inserted therein wire (within incorporating a variety of signal modifiers, e.g. buffers (col. 4, ll.44-48));

Claim 25: wherein the at least one wire is not a power supply line through which power is supplied to the semiconductor integrated circuit from a power supply (within plurality of signal paths (not power supply) (col. 5, l.6)).

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ulrey as applied to claim 12 above, and further in view of Thomas (US Patent 6,477,687).

With respect to claim 17 Ulrey teaches the limitation similar to the claim 12 including an apparatus to place and connect individual macro cells signals with traces that are supplemental to the macros cell layout. However Ulrey lacks the specifics regarding apparatus as a computer system including floor-planner. Thomas teaches:

a floor-planner comprising: an input section, a controller, and a display section, the input section providing inputs to a program in the controller that causes the display section to display a floorplan of a semiconductor device that includes a hard-macro (within floorplan editor, which is used by chip designer by placing macrocells to implement layout design including the ability of the editor to provide graphical feedback of the placed macros in the chip design including a display of routing and ability to correct/control routing (col. 1, ll.14-20)).

With respect to claim 18 Thomas teaches:

Claim 18: wherein the program analyzes a route of the wire (col. 1, ll.17-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mohan et al. to teach the specifics subject matter Ulrey dies not teach, because Another advantage of the present invention is increased circuit speeds because macrocells are disposed proximate to standard cells (col. 2, ll.26-28).

***Allowable Subject Matter***

9. Claims 6, 7, 20-24, 26 are allowed. The examiner's statement of reasons for allowance was indicated in the previous office action.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HR
06/18/2007

Helen Rossoshek
Examiner
Art Unit 2825